Parallel Control of a Class of Power Converters

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Abstract

The aim of this paper is to propose a class of parallel frequency-PWM control for quasi-resonant converters (QRC). The motivation of this control relies on the necessity of operating at both minimum energy losses (zero voltage or zero current switching) and minimum size conditions (high-frequency), which cannot be satisfied by frequency modulation or PWM alone. The proposed strategy is designed to provide robust stabilization in spite of model uncertainty and its performance is verified through an experimental application in a boost type QRC.

Keywords. Quasi-resonant converters, frequency control, PWM, parallel control.

1 Introduction

Electronic power processing has evolved around two fundamental techniques; namely, duty-cycle modulation or PWM and resonance. PWM-based converters have been widely used in the past because they are topological simpler and easier to operate with respect to resonance converters. By increasing switching frequency in PWM converters one might reduce the size of its magnetic components. This fact makes possible to operate PWM converters in order to satisfy optimal weight, size and cost conditions. On the other hand, operating at high frequencies results in more stressed switching devices, since semiconductors are forced to open at higher voltage and current conditions. Furthermore, the presence of leakage inductances in the transformer and junction capacitances in the semiconductor devices causes to power devices to inductively turn-off and capacitively turn on. As the semiconductor device switches off an inductive load, voltage spikes induced by the sharp time change of the current across the leakage inductances produce increased voltage stress and noise [1].

A common way to reduce switch stress and power loss in PWM converters is to add an LC resonant circuit to the semiconductor device. By doing so, the voltage (current) is forced to oscillate in a quasi-sinusoidal manner creating the zero current (ZCS) and zero voltage switching (ZVS) conditions. The resulting devices are the so-called quasi-resonant converters (QRC). In QRC, the LC circuit is used not only to shape the current and voltage waveform of the power switch but also to store and transfer energy from the circuit similar to conventional resonant converters. In this way, QRC are energetically more efficient than PWM converters. However, frequency modulation has the drawback of having limited load range and conversion ratio. In order to overcome this problem, one may try to convey the advantages of both control strategies by applying a mixed feedback control law that uses both frequency and duty-cycle of the switching device as control inputs. In principle, a feedback control strategy designed within this parallel structure would lead to a closed-loop system with moderated control actions and improved performance.

The aim of this brief paper is to propose a parallel feedback control strategy for QRC. One idea that will be exploited to deal with the usage of two control inputs to regulate a single output is to synthesize the feedback control by minimizing a criteria of performance that penalizes the deviation of the control actions from the nominal ones. The nominal control conditions are defined in order to convey the necessities of a reduced size and weight (high-frequency operation) and energy economy (ZVS or ZCS conditions). A systematic procedure of controller design is presented for any QRC and illustrated through an experimental application in a boost ZVS-QRC. The proposed strategy is shown to be of superior performance and robustness than the corresponding single-input control schemes.

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This brief paper is organized as follows. Section 2 describes the converter system and presents the control problem formulation. Section 3 introduces the parallel control of QRCs and Section 4 illustrates the performance of the controller via experimental work. Finally, in Section 5 some conclusions are presented.

2 Modelling and Control Problem Formulation

As stated above, the concept of resonant switch can be directly applied to conventional converters, which means that many topological variations of QRCs can be derived using the basic concept of zero voltage and zero current resonant switches. Since the first step in the controller design is the system modelling, for analysis purposes and due the great variety of QRC topologies, we will consider in this paper that the input-output (IO) dynamics of the converter can be described with a first-order model with a suitable dead-time as follows:

$$g(s) = \frac{k}{\tau s + 1}\exp(-\theta s) \tag{1}$$

where k is the system gain, $\tau > 0$ is a time-constant and $\theta > 0$ is the time-delay. Model parameters in (1) can be computed subjecting the power converter to a step perturbation on the operating conditions and characterizing its time response. The time-delay function $\exp(-\theta s)$ can be used to model either an authentic delayed process or an inverse response due to non-minimum phase dynamics (*i.e.*, right-hand zeroes) [2]. For $\theta = 0$, one has $g(s) = \frac{k}{\tau s+1}$ which corresponds to a first-order minimum-phase IO response. Typical examples of converters behaving in this way are buck, cuk and forward converters. On the other hand, converters with a right-hand zero include boost, buck-boost, flyback converters [3].

Let μ and f be respectively the duty-cycle and the frequency, and let V be the output voltage. If $\left(\overline{V}, \overline{\mu}, \overline{f}\right)$ the nominal operating point of the converter, one can introduce the deviation variables as follows: $y = V - \overline{V}$, $u_1 = \mu - \overline{\mu}$ and $u_2 = f - \overline{f}$. When both the duty-cycle and the frequency are defined as control inputs (parallel control) and the output voltage v is taken as the controlled output, the description of the IO system dynamics are given by the transfer function

$$y(s) = [G_{PWM}(s), G_{Freq}(s)]\begin{bmatrix} u_1(s) \\ u_2(s) \end{bmatrix} \tag{2}$$

Considering the converter dynamics (2), with $G_{PWM}(s)$ and $G_{Freq}(s)$ given as in (1), and y_d being a desired output voltage, the control problem can be stated as that of designing a feedback control law u to ensure stability of the controlled converter system and

$$\lim_{t\to\infty} y(t) = y_d \tag{3}$$

It is noticed that the nominal operating conditions $\overline{\mu}$ and $\overline{f}$ can be designed to satisfy certain operational requirements (*i.e.*, ZVS conditions and/or optimal size and weight).

3 Controller Synthesis

From (1) and (2), the IO system dynamics can be written as follows:

$$y = \frac{K_1}{\tau_1 s + 1}\exp(-\theta_1 s)u_1(s) + \frac{K_2}{\tau_2 s + 1}\exp(-\theta_2 s)u_2(s) \tag{4}$$

System (4) is a two-input and single-output (TISO) control system. The main idea that will be exploited below is to reduce the feedback control problem to a SISO one by imposing an additional constraint to close the additional degree-of-freedom present in the system (4). To this end, without lost of generality, assume that $\theta_1 \geq \theta_2$. In order to solve the control problem posed before, consider the converter dynamics represented in the following form:

$$y(s) = \frac{1}{\tau_1 s + 1}\exp(-\theta_1 s)w(s) \tag{5}$$

where

$$\begin{aligned} w(s) &= K_1 u_1(s) + K_2 c(s) \\ c(s) &= L(s)u_2(s) \\ L(s) &= \left(\tfrac{\tau_1 s+1}{\tau_2 s+1}\right)\exp(\theta_1 - \theta_2)s \end{aligned} \tag{6}$$

The operator $L(s)$ has the following properties: a) The function $L(s)$ is invertible in the sense that $L(s)^{-1}$ is a causal operator. In other words, given the signal $c(s)$, one can compute the actual control input $u_2(s)$ just by taking $u_2(s) = L(s)^{-1}c(s)$. b) $L(0) = 1$. This means that, at steady-state conditions, $u_2 = c$.

To obtain the parallel control design, the following procedure is proposed:

1. System (5) is a stable first-order with time-delay SISO system. Use the a classical PI compensator

$$w(s) = K_{c,w}\left[1 + \frac{1}{\tau_{I,w} s}\right]e_y(s) \tag{7}$$

to regulate the output voltage error $e_y = y_d - y = V_d - V$. There exist in the literature several rules and guidelines for tuning control law (7) (see, for instance, D'Azzo and Houpis [2], Morari and Zafirou [4]). The tuning of controller (7) will define the stability and performance characteristics of the overall closed-loop system. In particular, connections between linear PI controller and robust control has been studied by Morari and Zafiriou [4] deriving the so-called internal model control (IMC). The motivation behind IMC design procedures is the necessity of guaranteeing both disturbance rejection and acceptable performance of the closed-loop system. Specifically, the IMC tuning rules for the PI controller (7) in terms of the parameters of the system (5) are

$$\begin{aligned} K_{c,w} &= \tau_1/\left(\tau_c+\theta\right) \\ \tau_{I,w} &= \tau_1 \end{aligned} \tag{8}$$

where τ_c is the desired closed-loop time-constant. As an heuristic rule, choose τ_c of the order of 0.5 to 0.75 times the open-loop time-constant τ_1. Notice that the presence of the time-delay $\exp(-\theta_1 s)$ limits the value of the maximum achievable controller gain $K_{c,w}$; indeed, $K_{c,w} < \tau_1/\theta$. If the non-controlled converter is poorly damped, a common practice is to add a current feedback to enhance the transient properties of the controlled circuit. This results in the so-called current-mode control. In the way, the compensator becomes

$$w(s) = K_{c,w}\left[1+\frac{1}{\tau_{I,w}s}\right]e_y(s)+K_{ci}e_i(s) \tag{9}$$

where K_{ci} is the gain of the current loop, $e_i = \bar{i} - i$, i is the current and $\bar{i}$ is the nominal operating value of the current.

2. The system input $w(s)$ given as in step 1 ensures the stability of the closed-loop system and the asymptotic tracking of the desired output y_d [4]. Considering that $w(s)$ is given by the sum $K_1u_1(s)+K_2c(s) = K_1u_1(s)+K_2L(s)u_2(s)$, a procedure to divide w between u_1 and u_2 is required. The following optimization problem is posed:

$$\min\frac{1}{2}\left[\alpha\left(K_1u_1(s)\right)^2+(1-\alpha)\left(K_2L(s)u_2(s)\right)^2\right] \tag{10}$$

subjected to the constraint

$$K_1u_1(s)+K_2L(s)u_2(s) = w(s) \tag{11}$$

where $0 \le \alpha \le 1$ is a constant that weights the role of the "inputs" $K_1u_1(s)$ and $K_2L(s)u_2(s)$. By noticing that $K_1u_1(0)$ and $K_2u_2(0)$ are the steady-state components of the controlled output (*i.e.*, from (4) one has that $y(0) = K_1u_1(0)$ and $K_2u_2(0)$), the idea behind the index function (10) is to minimize the *steady-state* contributions of the control inputs u_1 and u_2. In fact, since $L(0) = 1$, at steady-state one has that the index function (10) becomes $\frac{1}{2}\left[\alpha\left(K_1u_1(0)\right)^2+(1-\alpha)\left(K_2u_2(0)\right)^2\right]$. The constant α plays an important role in the optimization problem (10)-(11): If $\alpha = 0$, then $u_2(s) = 0$ and the frequency is set at its nominal value $\bar{f}$. Or alternately, when $\alpha = 1$, then $u_1(s) = 0$ and the duty cycle is set at its nominal value $\bar{\mu}$. In this way, if $0 < \alpha < 1$ both control inputs u_1 and u_2 have non-trivial contributions to the control of the converter. By using Lagrange operator methods [5], the optimization problem (10)-(11) leads to the following expressions for $u_1(s)$ and $u_2(s)$:

$$\begin{aligned} u_1(s) &= (1-\alpha)K_1^{-1}w(s) \\ u_2(s) &= \alpha K_2^{-1}L(s)^{-1}w(s) \end{aligned} \tag{12}$$

As discussed above, notice that $u_1(s) = 0$ (respectively $u_2(s) = 0$) is $\alpha = 0$ (respectively $\alpha = 1$). Besides, for $\alpha \neq 1$ the control input $u_2(s)$ is well-defined since the inverse $L(s)^{-1}$ a causal (*i.e.*, realizable) operator. In this way, the control input $u_2(s)$ is computed in the following form:

$$u_2(s) = \alpha K_2^{-1}\left(\frac{\tau_2 s+1}{\tau_1 s+1}\right)\exp\left(-\theta_{12}s\right)w(s) \tag{13}$$

where $\theta_{12} = \theta_1 - \theta_2 \ge 0$. Notice that the control input $u_2(s)$ is delayed, with delay $\theta_{12} \ge 0$, with respect to the signal $w(s)$. Such delay is required to synchronize the control inputs u_1 and u_2. In this way, the stabilization of the TISO system (4) is limited mainly by the larger delay. A schematic diagram of the proposed controller is shown in Figure 1.

The following can be remarked:

- Parallel control has an additional advantage over the single input control scheme; namely, it can deal better with input saturation. When the control input has integral action and the system is subjected to disturbances, the control action might saturate. Saturation of integral actions can lead to the well-known phenomenon of "wind-up". In the single control scheme, wind-up may be the cause of a severe performance deterioration or even instability. In the parallel control scheme, the saturations of one control signal can be compensated with the other control input, being able to regulate the output effectively.

- The control strategy developed in this paper can be applied to high-power quasi-resonant converters also. In fact, the operation of high-power converters is mainly hampered by two factors: a) energy dissipation and heat generation and b) its highly nonlinear behavior. From the control viewpoint, moderate heat generation actually would help to obtain a better closed-loop performance, since this energy dissipation can be seen as an additional damping injected to the system. On the other hand, as stated before, the nonlinear behavior of the system can be compensated more efficiently using the two-input control scheme.

4 An Illustrative Example

The objective of this section is two-fold: i) to illustrate the functioning of the controller and ii) to evaluate the controller performance. The experimental implementation of the controller was carried out in a boost ZVS-QRC (see Figure 2) with the following parameters [3]: $L_r = 60\ \mu H$, $C_r = 10\ nF$, $L_o = 1.2\ mH$, $C_o = 0.42 nF$, $V_g = 5\ volt$ and $R = 64\Omega$. As stated above, a IO model of the system can be performed by subjecting the inputs to a step disturbance. By doing so, the following parameters of the transfer functions were obtained: $K_1 = -6.5\ volt$, $K_2 = -1.05 \times 10^{-5}\ volt/Hz$, $\theta_1 = 0.00376$ sec and $\theta_2 = 0.0045$ sec, $\tau_1 = 0.098$ sec and $\tau_2 = 0.053$ sec. According to model parameters and using IMC tuning guidelines the PI gains of the controller (9) were chosen as: $K_{c,w} = 0.1\ volt$ and $\tau_{I,w} = 0.03$ sec. Furthermore, a current-mode control was used to add damping and the proportional current action was chosen such that $K_{c,i} = 0.1\ amp$. The following nominal values were used: $\overline{\mu} = 0.45$, $\overline{f} = 125\ KHz$. The latter corresponds to 0.6 times the natural resonant frequency of the circuit. The control algorithm was executed on a PC-based real-time control platform and the sample period was 1 ms.

To illustrate the functioning of the controller, it is required to follow a square-wave reference signal (from 6 $volt$ to 8 $volt$). Initially, the control actions are performed exclusively by frequency modulation. At time $t = 4.5$ sec, both frequency and duty-cycle modulation are used. The results are shown in Figure 3. Notice that the control effort due to frequency input is considerable reduced after the activation of the duty cycle as the second control input. Notice also that the performance of the closed-loop system is considerable improved, yielding a smoother tracking of the reference signal. Thus, parallel control leads to less demanding control signals and to performance improvement.

The capacity of the controller to deal with input saturation is illustrated in Figure 4. In this case, a comparison of the performance between the single-input scheme and parallel scheme is presented. In Figure 4 the duty cycle control input is suddenly saturated at $t = 5.3$ sec ($\mu = 0.3$). Notice that in spite of this saturation, the frequency input is able to regulate the output voltage at the required level.

The robustness and performance of the proposed controller in face of load changes is illustrated in Figure 5. In this case, a load change of about 20% occurs at $t = 4.0$ sec ($R = 52\ \Omega$). It can be observed that the proposed controller is able to regulate the output voltage even in the case of significative parameter disturbances by modulating both the duty cycle and the operation frequency.

5 Conclusions

This paper has addressed the voltage regulation problem of QRC using parallel control (two control inputs for a single control objective). The proposed controller is designed by minimizing a criteria, which balances the usage of the control inputs. This fact makes the controller able to operate in both minimum power loss and high-frequency regions. Experimental evidence has shown that the proposed controller can deal better with input saturation than single-input schemes. Besides, the proposed two-input controller in a boost ZVS-QRC has shown that the control law provides stability and acceptable system performance.

6 References

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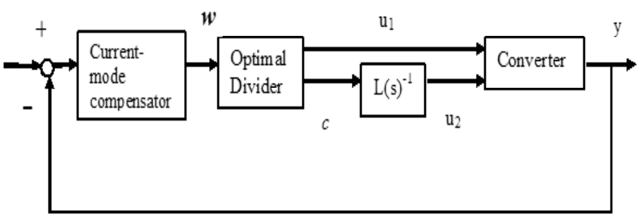

Figure 1. Schematic diagram of parallel control.

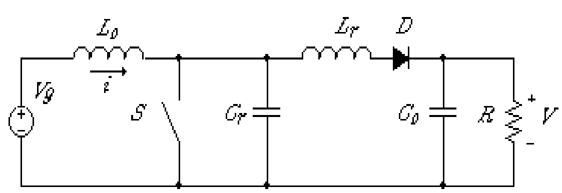

Figure 2. Boost ZVS-QRC.

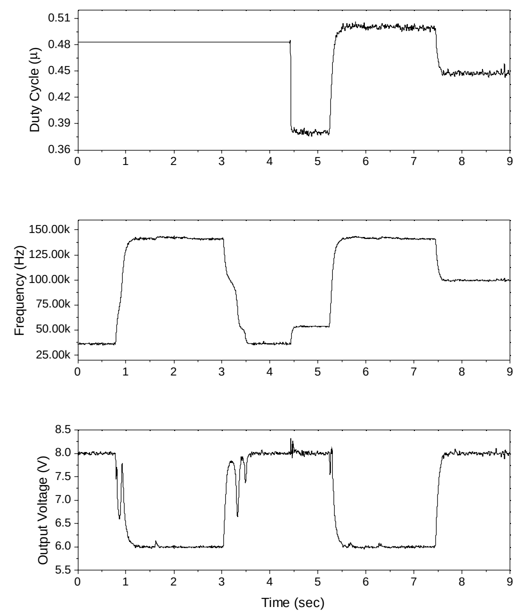

Figure 3. Time evolution of the converter under a) ($t < 4.5\,\mathrm{sec}$) single input control law b) ($t \geq 4.5\,\mathrm{sec}$) parallel control.

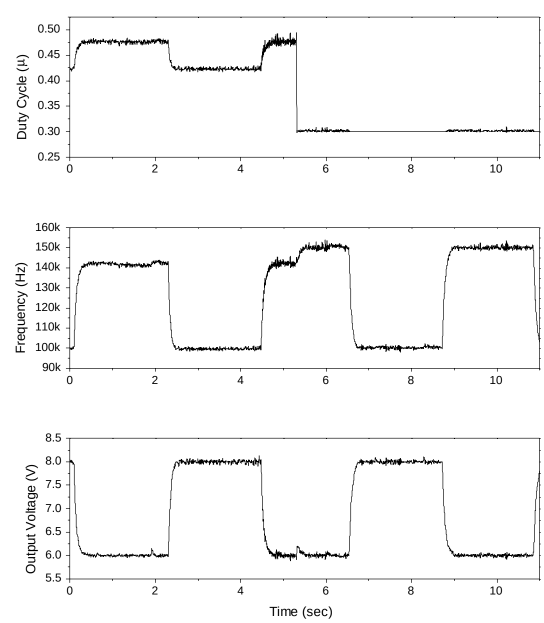

Figure 4. Time evolution of the converter under parallel control, at time $t = 5.3\,\mathrm{sec}$ the duty-cycle input saturates.

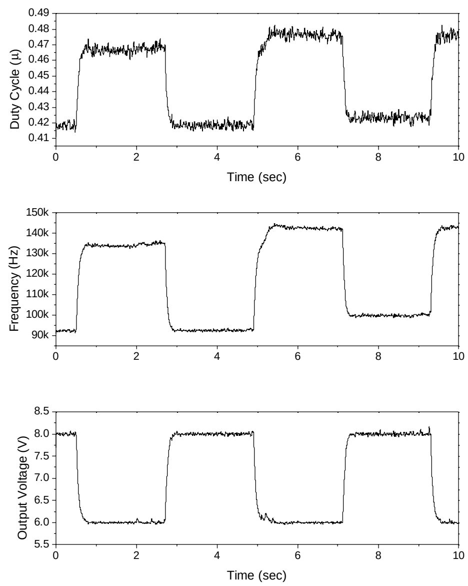

Figure 5. Time evolution of the converter under parallel control when a load disturbance occurs at $t = 4\,\mathrm{sec}$.